Product Name	GAOTek Ultra-Low-Power MCU
Product SKU	GAOTek-IDK-299
Product URL	https://gaotek.com/product/gaotek-ultra-low-power-mcu/

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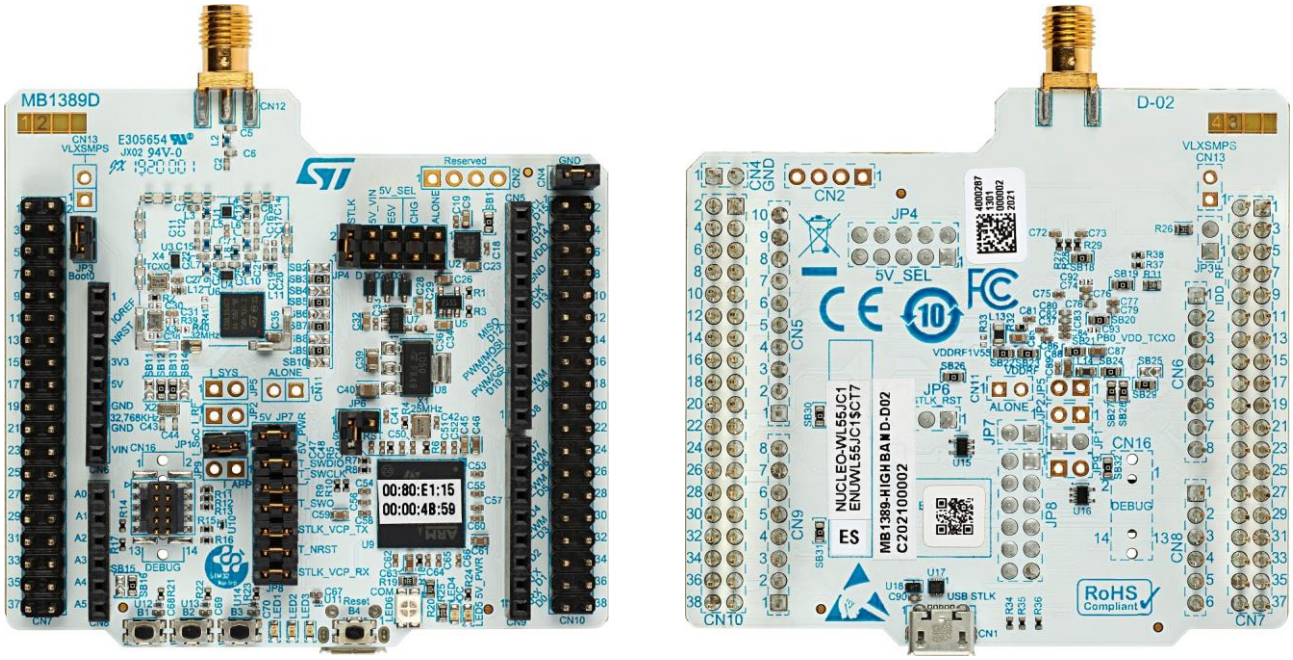
Contents

1. Introduction

The product, based on the MB1389 reference board provides an affordable and flexible way for users to try out new concepts and build prototypes with the series microcontroller, choosing from the various combinations of performance, power consumption, and features.

The Uno V3 connectivity support and the ST morpho headers provide an easy means of expanding the functionality of the open development platform with a wide choice of specialized shields. The Nucleo-64 board does not require any separate probe as it integrates the STLINK-V3E debugger and programmer.

The Nucleo-64 board is provided with the comprehensive software HAL library and various packaged software examples available with the STM32CubeWL MCU Package.



2. Development environment

2.1. System requirements

- Multi-OS support: Windows® 10, Linux® 64-bit, or macOS®
- USB Type-A or USB Type-C® to Micro-B cable

Note: macOS® is a trademark of Apple Inc. registered in the U.S. and other countries. Linux® is a registered trademark of Linus Torvalds. All other trademarks are the property of their respective owners.

2.2 Development toolchains

- IAR Systems® - IAR Embedded Workbench® (1)
- Keil® - MDK-ARM (1)
- STMicroelectronics - STM32CubeIDE

1.On Windows® only.

2.3. Demonstration software

The demonstration software, included in the STM32Cube MCU Package corresponding to the on-board microcontroller, is preloaded in the STM32 Flash memory for easy demonstration of the device peripherals in standalone mode.

3. Conventions

Table 3 provides the conventions used for the ON and OFF settings in the present document.

Table 3. ON/OFF convention

Convention	Definition
Jumper JPx ON	Jumper fitted
Jumper JPx OFF	Jumper not fitted
Jumper JPx [1-2]	Jumper fitted between Pin 1 and Pin 2
Solder bridge SBx ON	SBx connections closed by 0 Ω resistor
Solder bridge SBx OFF	SBx connections left open
Resistor Rx ON	Resistor soldered
Resistor Rx OFF	Resistor not soldered

4. Quick start

The Nucleo-64 board is an easy-to-use and low-cost development kit used to evaluate and start development quickly with a Series microcontroller in the UFBGA73 package. Before installing and using the product, accept the Evaluation Product License Agreement.

4.1 Getting started

Follow the sequence below to configure the Nucleo-64 board and launch the demonstration application (refer to Figure 4 for component location):

1. Check jumper positions on board, JP1 (I_SoC) ON, JP3 (BOOT0) ON, JP4 (Power source) on 5V_USB_STLK, JP7 (5V_PWR) ON, and JP8 all 6 jumpers ON. The jumper position on the board is explained in Table 4.

2. Connect the Nucleo-64 board to a PC with a standard USB cable through the CN1 USB connector to power the board. Then the LED5 (PWR) green LED and the LED6 (COM) LED light up, the three LED1, LED2, and LED3 LEDs blink.

3. On the PC, connect a UART terminal to the board using the following settings:
   - UART terminal: new line received = auto; new line transmits = LF (line feed)
   - Serial port setting: select COM port number, 9600 baud rate, 8-bit data, parity none, 1 stop bit, no flow control

4. Press on the B4 Reset button of the Nucleo-64 board.
   - The Nucleo-64 board remains silent until it gets a command from the connected PC to start sending a beacon on one of the beacon frequencies.
   - The frequency is selected depending on the region.
   - After the version check, the first three commands to send to the PC must set region, subregion, and start the beacon (AT+REGION=x and AT_BEACON_ON). The first two commands select the format of the transmission beacon. The third command starts sending the beacon.
   - For a list of available regions run AT_LIST_REGIONS.

5. Then the concentrator (a second NUCLEO-WL55JC) starts flashing a green LED on each time slot of the network.

6. To get the demonstration fully up and running, up to 14 Nucleo demonstration sensors can be flashed and placed against a Nucleo demonstration concentrator.

Table 4. Jumper configuration

Jumper	Definition	Position (1)	Comment (1)

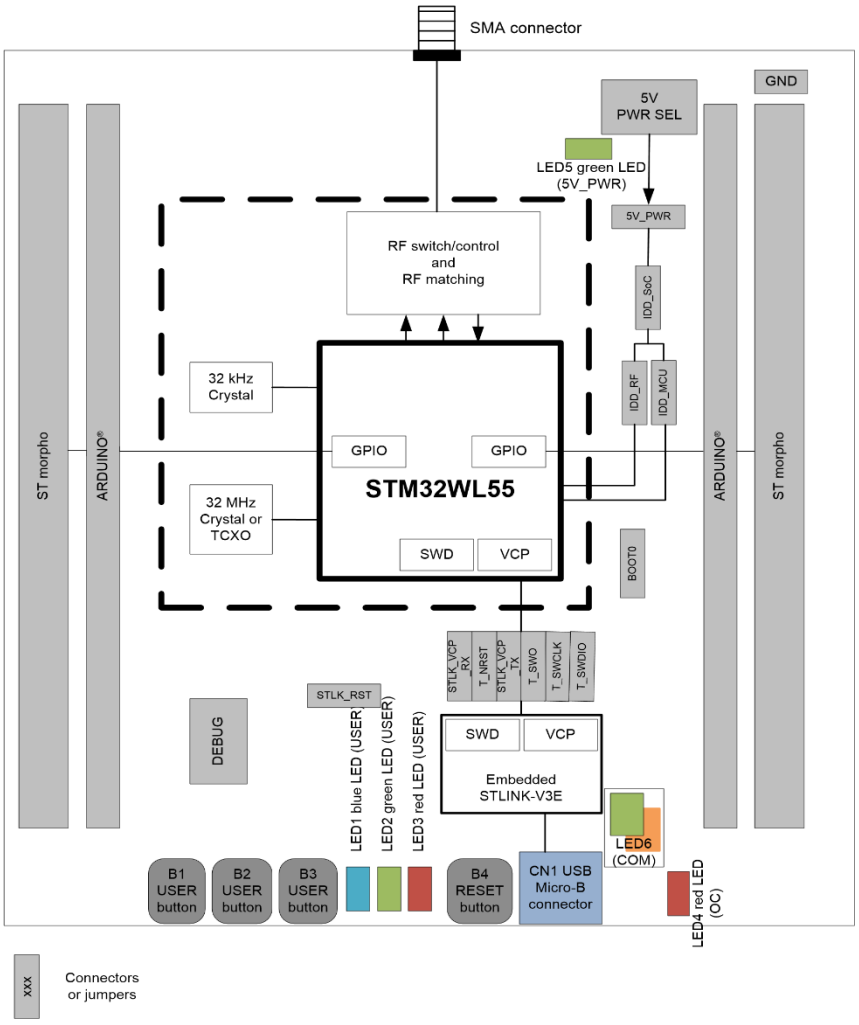
JP1	I_SoC	ON	For current measurements
JP2	I_RF	OFF (SB28 ON)	For current measurements (RF part)
JP3	BOOT0	ON	Allows to disconnect PH3/ BOOT0 pull-down resistor and to use it as an I/O if the software BOOT0 is used, thanks to the option bytes.
JP4	5 V power-source selection	[1-2] (Default)	5V_USB_STLK (from ST-LINK)
		[3-4] (optional)	5V_VIN
		[5-6] (optional)	E5V
		[7-8] (optional)	5V_USB_CHGR
		[9-10] (optional)	STD_ALONE_5V

Jumper	**Definition**	**Position** (1)	**Comment** (1)
JP5	I_SYS	OFF (SB27 ON)	For current measurements (Digital part)
JP6	STLK-RST	OFF	STLINK-V3E reset
JP7	5V_PWR	ON	5 V power-source selection
JP8	Signals between STLINK-V3E and MCU target	[1-2]	T_SWDIO connected to ST-LINK
		[3-4]	T_SWCLK connected to ST-LINK
		[5-6]	T_SWO connected to ST-LINK
		[7-8]	STLK_VCP_TX connected to ST-LINK
		[9-10]	T_NRST connected to ST-LINK
		[11-12]	STLK_VCP_TX connected to ST-LINK
JP9	I_APP	OFF (SB32 ON)	For U3 and U4 DC switches current measurement

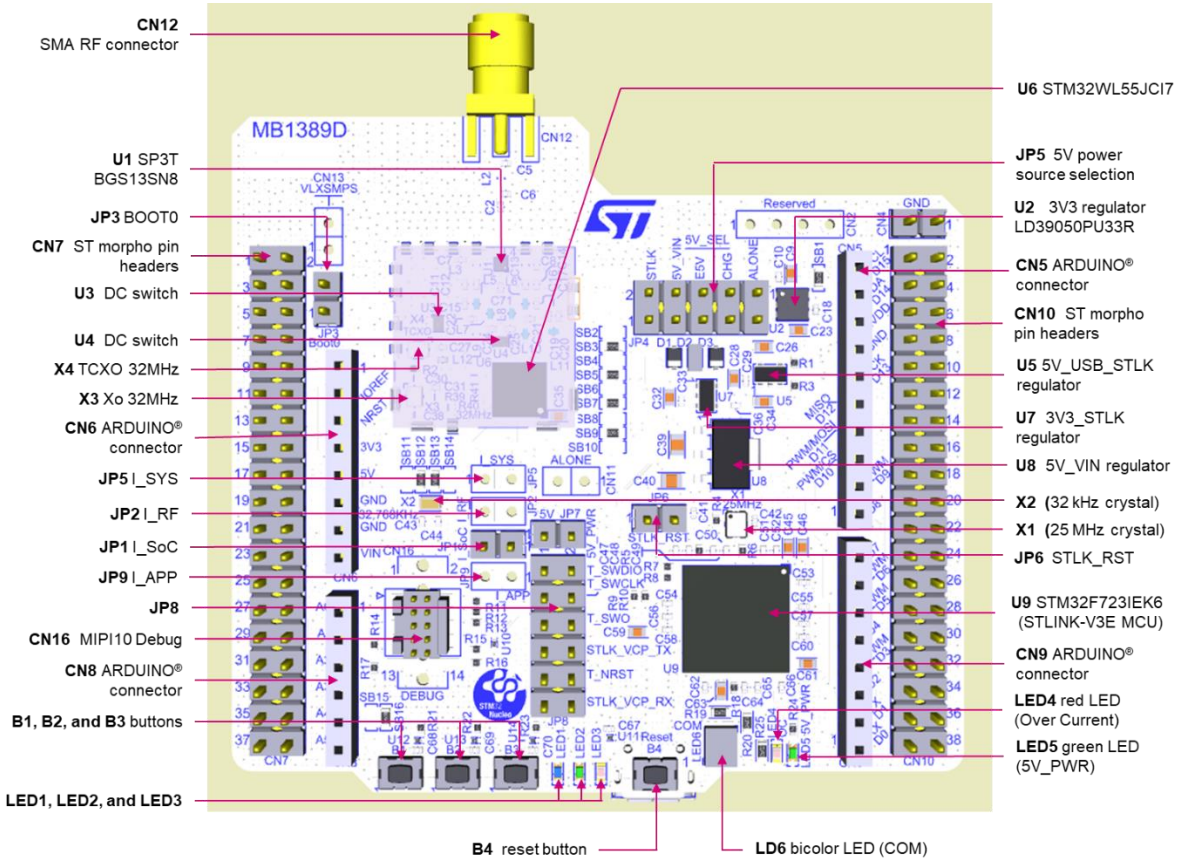
5. Hardware layout and configuration

The Nucleo-64 board is designed around the STM32 microcontrollers in a 73-pin UFBGA package. Figure 3 shows the connections between the STM32 and its peripherals (STLINK-V3E, push - buttons, LEDs, USB, Uno and ST morpho headers). Figure 4 and Figure 6 show the location of these features on the Nucleo-64 board. The mechanical dimensions of the board are shown in Figure 7.

Figure 3. Hardware block diagram



5.1 PCB layout



Two stickers are present on the top of the board: one RF certification sticker and one UID64 sticker.

1. The RF certification sticker is mandatory for any boards containing an RF module as this product, which contains a RF transceiver. This sticker is placed on top of the RF shielded box. This sticker must have a maximum size of 16 mm x 16 mm. This sticker displays at least the product CPN (NUCLEO-WL55JCx), the board reference (MB1389x-0x), the FCC ID number (YCP-MB1389000), the ISED ID (8976A-MB1389000) of the board, and the CE logo.

2. The UID64 sticker. A 64-bit unique device identification (UID64) is stored in the Flash memory and can be accessed by the CPUs, at the 0x1FFF7580 base address. The UID64

sticker (with a size of 10 mm x 5 mm) displays the UID information (16 digits as 64-bit codification in little-endian byte order) which is unique for each LoRa MCU, so unique for each MB1389 board.

Figure 5 shows both stickers:

Figure 5. RF certification and UID64 stickers

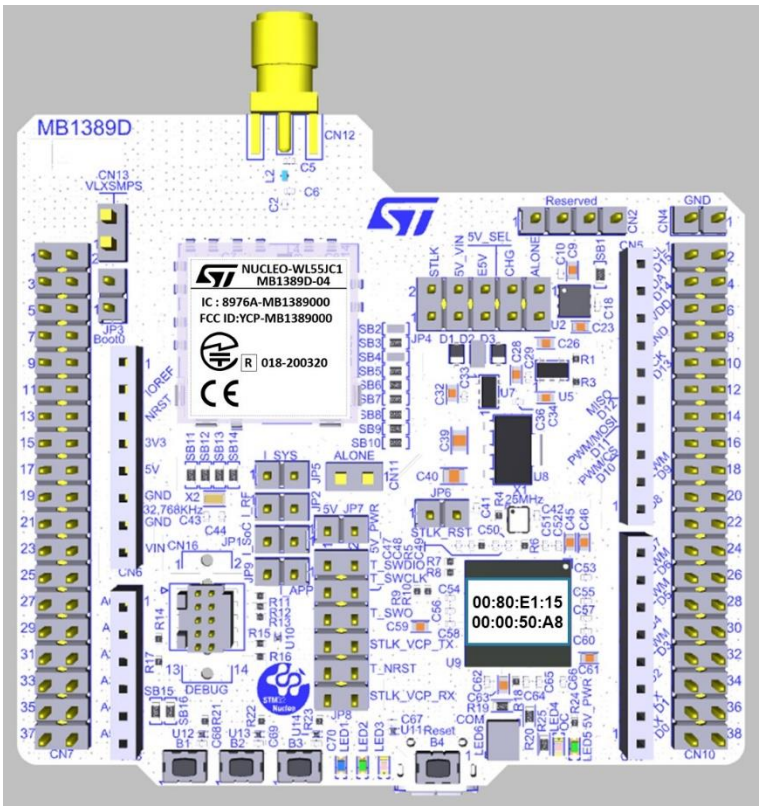
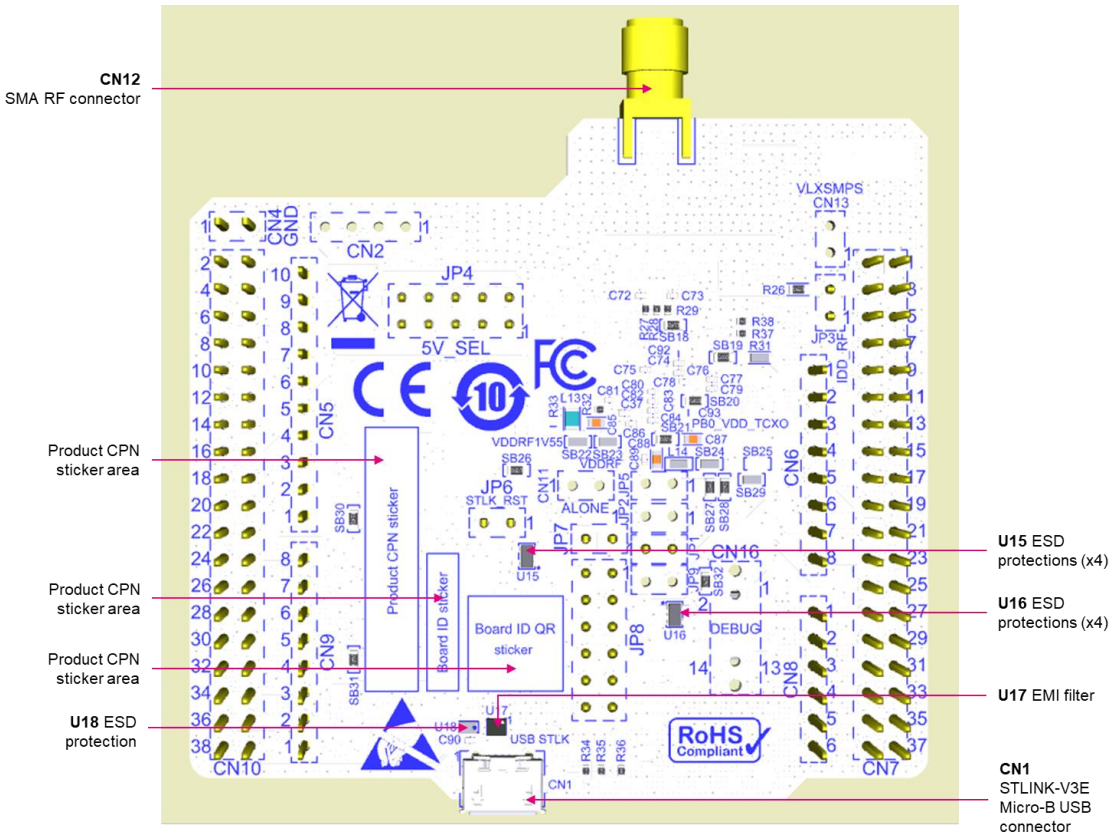
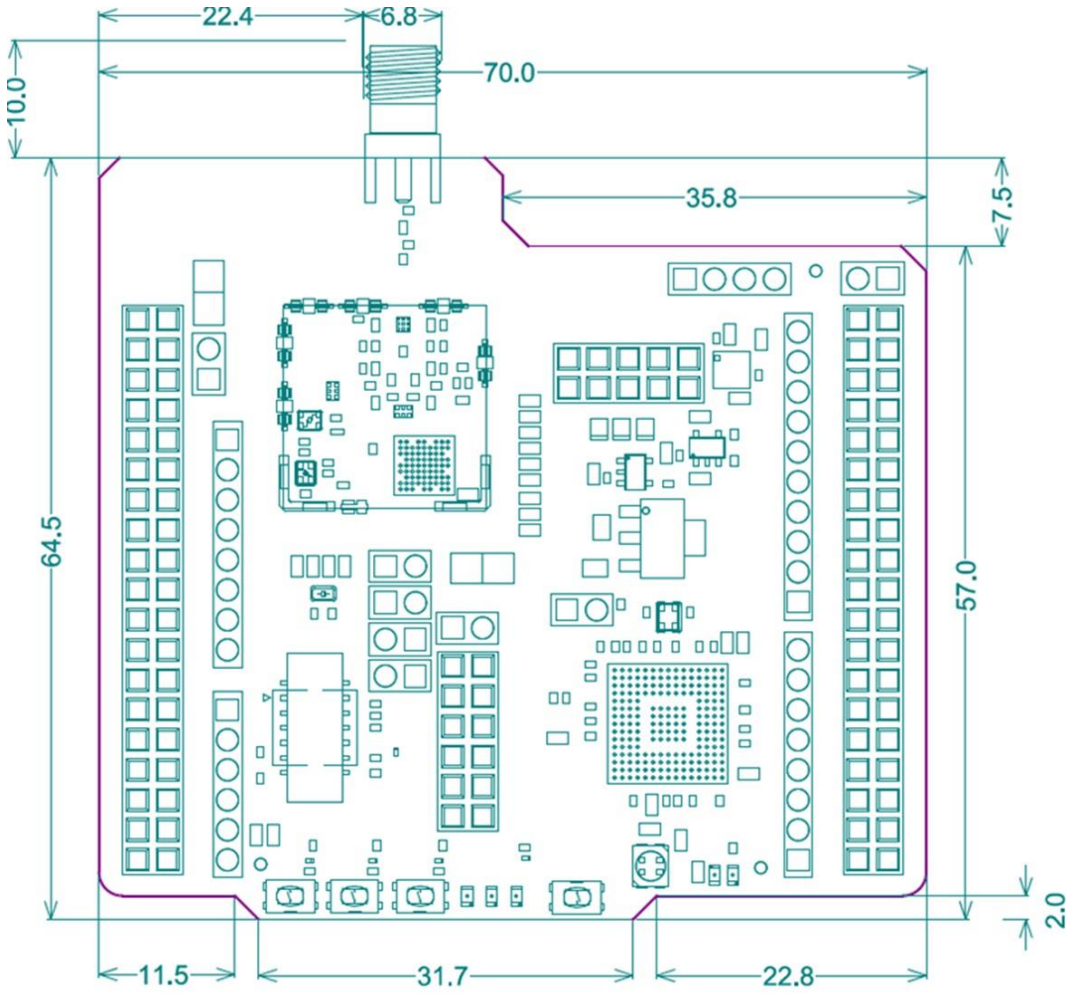


Figure 6. Bottom layout



5.2 Mechanical drawing

Figure 7. board mechanical drawing (in millimeter)



5.3 Embedded

There are two different ways to program and debug the onboard STM32 MCU:

- Using the embedded.
- Using an external debug tool connected to the CN16 MIPI10 connector.

The programming and debugging tool are integrated into the Nucleo-64 board. The embedded supports only SWD and VCP for STM32 devices. For information about debugging and programming features of STLINK-V3, refer to the user manual STLINK-V3SET debugger/programmer for STM8 and STM32 (UM2448), which describes in detail all the STLINK-V3 features.

Features supported on STLINK-V3E:

- 5 V power supplied by CN1 USB connector.
- USB 2.0 high-speed-compatible interface.
- SWD JTAG/serial wire debugging specific features:
  - 3 to 3.6 V application voltage on the JTAG/SWD interface and 5 V tolerant inputs.
  - JTAG.
  - Serial viewer communication.
- CN16 MIPI10 connector
- LED6 COM status LED blinking during communication with the PC
- LED4 OC fault red LED alerting on USB overcurrent request
- U4 5 V / 300 mA output power supply capability with current limitation and LED
- LD4 5V_PWR 5 V power green LED

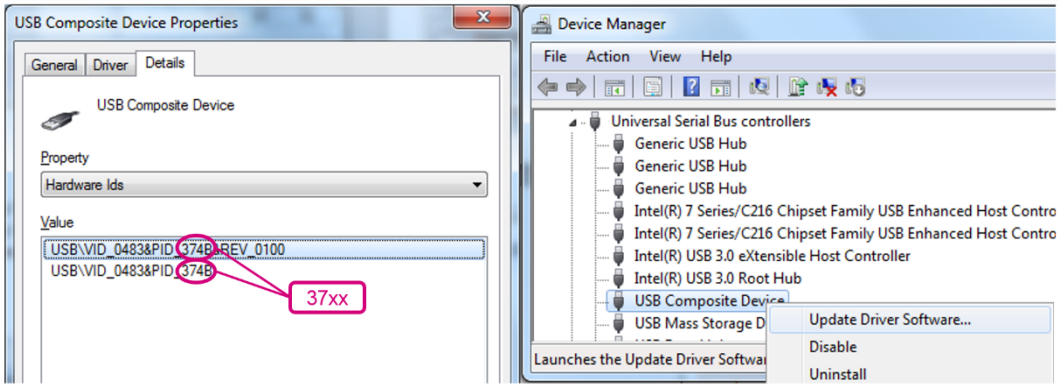
5.3.1 Drivers

Before connecting the Nucleo-64 board to a Windows 7®, Windows 8®, or Windows 10® PC via USB, a driver for the STLINK-V3E (stsw-link009) must be installed (not required for Windows 10®). It is available on the website.

In case the Nucleo-64 board is connected to the PC before the driver is installed, some Nucleo-64 interfaces may be declared as Unknown in the PC device manager. In this case, the user must install the dedicated driver files, and update the driver of the connected device from the device manager as shown in Figure 8.

Note: Prefer using the USB Composite Device handle for a full recovery.

Figure 8. USB composite device



Note:37xx:

- 374E for STLINK-V3E without bridge functions
- 374F for STLINK-V3E with bridge functions

5.3.2 STLINK-V3E firmware upgrade

The STLINK-V3E embeds a firmware upgrade mechanism for the in-situ upgrade through the USB port. As the firmware may evolve during the lifetime of the STLINK-V3E product (for example new functionalities, bug fixes, support for new microcontroller families), it is recommended to visit the www.st.com website before starting to use the Nucleo-64 board and periodically, to stay up-to-date with the latest firmware version.

5.3.3 Using an external debug tool to program and debug the on-board STM32

There are two basic ways to support an external debug tool:

1. Keep the embedded STLINK-V3E running. Power on the STLINK-V3E at first until the COM LED turns red. Then connect the external debug tool through the CN16 STDC14/MIPI-10 debug connector.

2. Set the embedded STLINK-V3E in a high-impedance state. When the STLK_RST JP6 jumper is ON, the embedded STLINK-V3E is in RESET state and all GPIOs are in high impedance. Then, connect the external debug tool to debug connector CN16.

Figure 9. Connecting an external debug tool to program the on-board

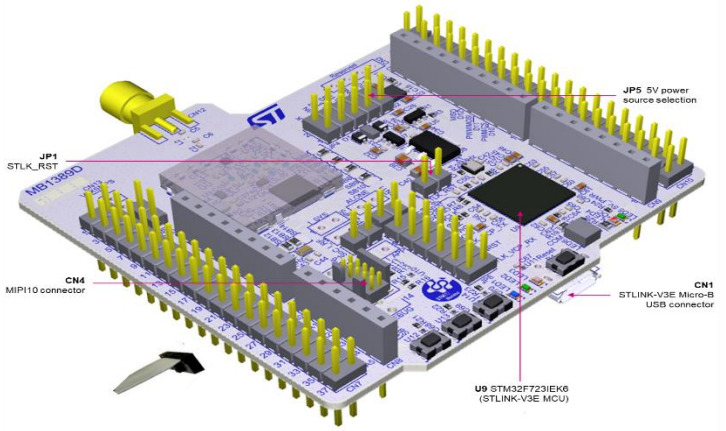


Table 5. CN16 MIPI10 / STDC14 debug connector

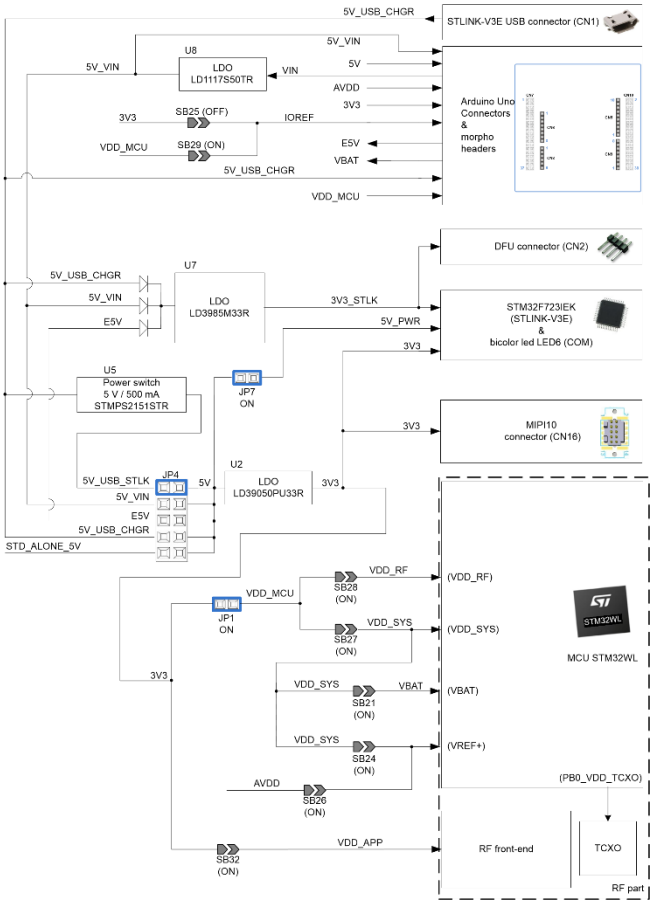
MIPI10 pin	STDC14 pin	CN4	Function
-	1	NC	Reserved
-	2	NC	Reserved
1	3	3V3	Target VCC
2	4	T_SWDIO	T_JTMS target SWDIO using SWD protocol or Target JTMS using JTAG protocol
3	5	GND	Ground
4	6	T_SWCLK	T_JCLK target SWCLK using SWD protocol or Target JCLK using JTAG protocol
5	7	GND	Ground
6	8	T_SWO	T_JTMS target SWO using SWD protocol or Target JTDO using JTAG protocol
7	9	NC	Not connected
8	10	T_JTDI	T_JTDI not used by SWD protocol, Target JTDI using JTAG protocol, only for external tools
9	11	GNDDetect	GND detect for plug indicator, used on SWD and JTAG neither
10	12	T_NRST	T_JTMS target NRST using SWD protocol or Target JTMS using JTAG protocol
-	13	T_VCP_RX	Target RX used for VCP, from UART dedicated to bootloader
-	14	T_VCP_TX	Target TX used for VCP, from UART dedicated to bootloader

5.4 Power supply

The power supply can be provided by six different sources:

- A host PC connected to CN1 through a USB cable (default setting).
- An external VIN from 7 to 12 V power supply connected to CN7 pin 24.
- An external E5V 5 V power supply connected to CN7 pin 6.
- An external 5V_USB_CHGR 5 V USB charger connected to CN1.
- An external 3V3 3.3 V power supply connected to CN7 pin 16.
- An external STD_ALONE_5V 5 V power supply to supply only the MCU part and not the STLINK-V3E part.

Figure 10. Nucleo-64 board power tree

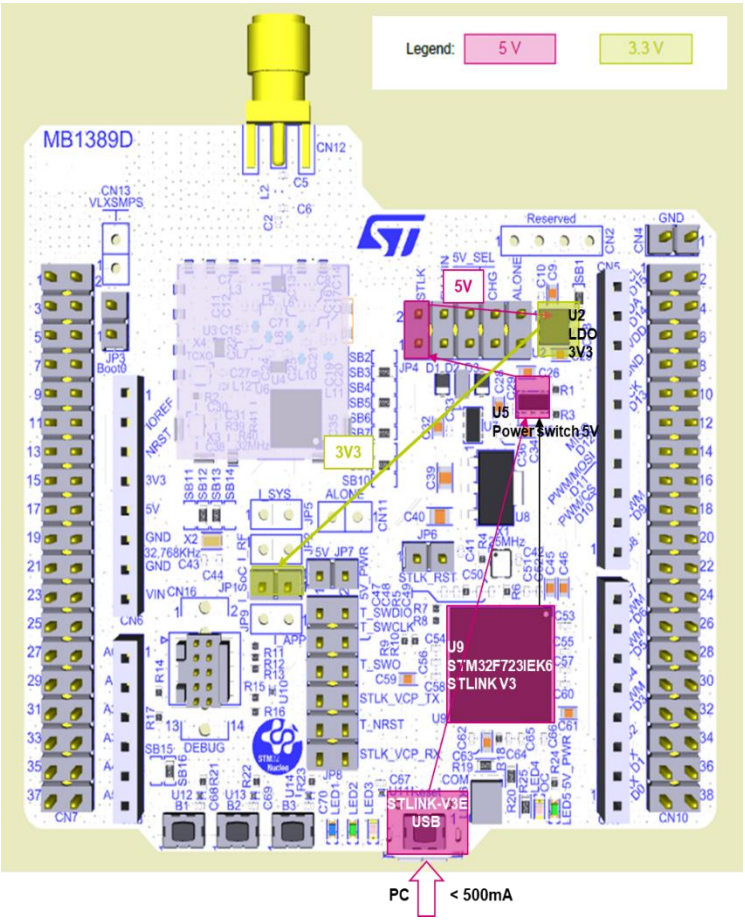


In case 5V_VIN, E5V, 5V_USB_CHGR, 3V3, or STD_ALONE_5V is used to power the Nucleo-64 board, this power source must comply with the EN-60950-1: 2006+A11/2009

standard and must be Safety Extra Low Voltage (SELV) with limited power capability. If the power supply is 3V3 or STD_ALONE_5V, the ST-LINK is not powered and cannot be used. Power supply input from STLINK-V3E USB connector (default setting)

The Nucleo-64 boar and shield can be powered from STLINK-V3E connector CN1 (5 V) by setting 5V_SEL jumper JP4 [1-2] on STLK, as illustrated in Figure 11. This is the default setting.

Figure 11. Power supply input from STLINK-V3E USB connector with PC (5 V, 500 mA maximum)



If the USB enumeration succeeds, the 5V_USB_STLK power is enabled, by asserting the T_PWR_EN signal from U9 STLINK-V3 STM32F723IEK6. This pin is connected to the

U5 STMPS2151STR power switch, which powers the board. The U5 STMPS2151STR power switch features also a current limitation to protect the PC in case of a short-circuit on board. If an overcurrent higher than 500 mA occurs on board, the LED4 red LED is lit.

The board and its shield can be powered from ST-LINK USB connector CN1, but only the ST-LINK circuit gets power before USB enumeration because the host PC only provides 100 mA to the board at that time.

During the USB enumeration, the board requires 500 mA power from the host PC.

- If the host can provide the required power, the enumeration finishes by a Set Configuration command and then, the power switch STMPS2151STR is switched ON, the 5V_PWR LED5 green LED is turned ON, thus the board and its shield on it can consume 500 mA at the maximum.
- If the host is not able to provide the requested current, the enumeration fails. Therefore, the U5 power switch STMPS2151STR remains OFF and the MCU part including the extension board is not powered. As a consequence, the LED5 green LED remains turned OFF. In this case, it is mandatory to use an external power supply.

Caution: If the maximum current consumption of the Nucleo-64 board and its shield boards exceeds 300 mA, it is mandatory to check the root cause of the overconsumption, and consequently, if needed, to power the Nucleo-64 board with an external power supply connected to VIN, 5 V or 3.3 V.

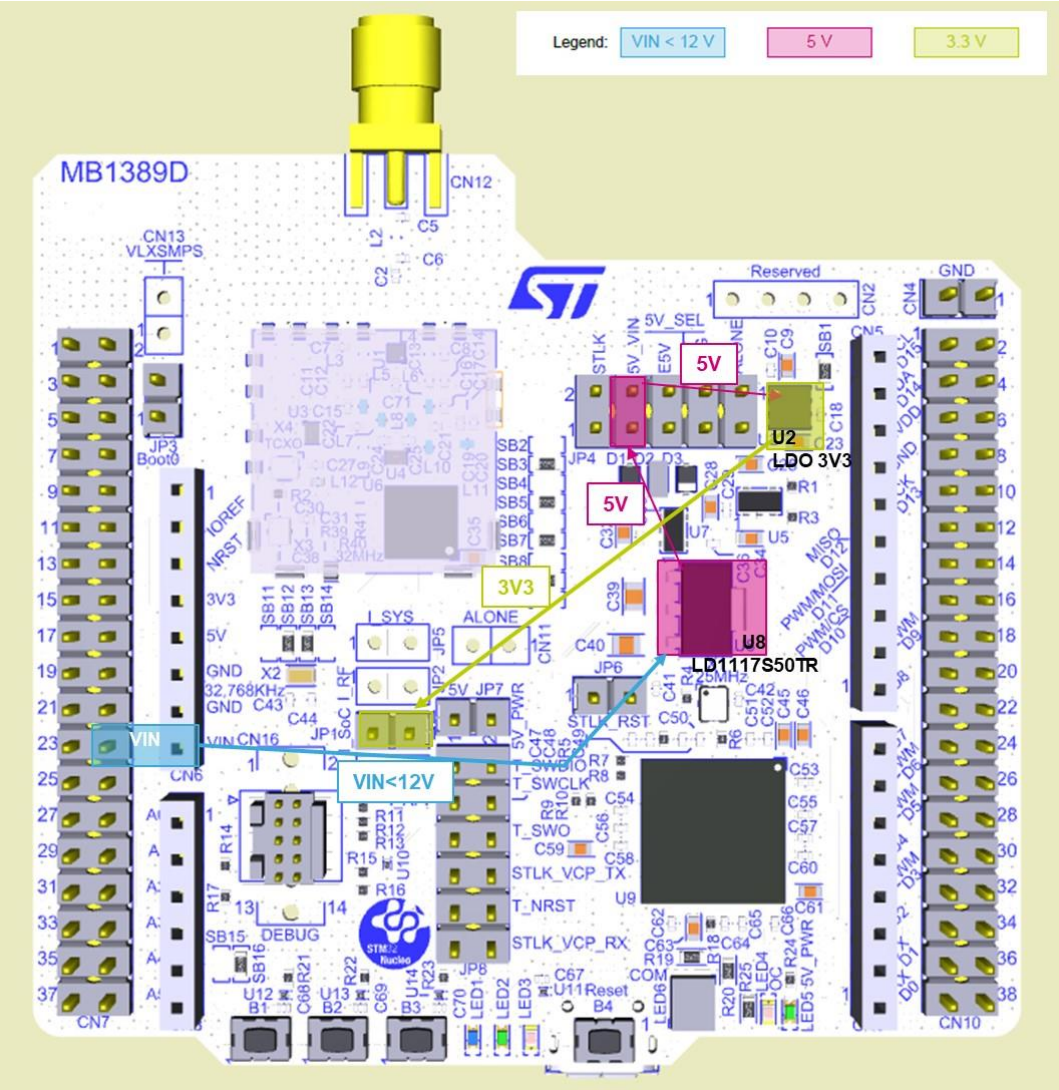
- External power supply input from VIN (7 to 12 V, 800 mA maximum)
- When the Nucleo-64 board is power-supplied by VIN (refer to Table 6 and Figure 12), the jumper configuration must be the following: jumper JP4 [3-4] on 5V_VIN.
- The Nucleo-64 board and its shield boards can be powered in three different ways from an external power supply, depending on the voltage used. The three cases are summarized in Table 6.

Table 6. External power sources: VIN (7 to 12 V)

Input power name	Connector pins	Voltage range	Maximum current	Limitation
VIN	CN6 pin 8 CN7 pin 24	7 to 12 V	800 mA	From 7 to 12 V only and input current capability is linked to input voltage: • 800 mA input current when VIN = 7 V • 450 mA input current when 7 V < VIN < 9 V • 250 mA input current when 9 V < VIN < 12 V

Refer to Section 6.4.1 for debugging when using an external power supply.

Figure 12. Power supply input from VIN (7 to 12 V, 800 mA maximum)



External power supply input from E5V (5 V, 500 mA maximum).

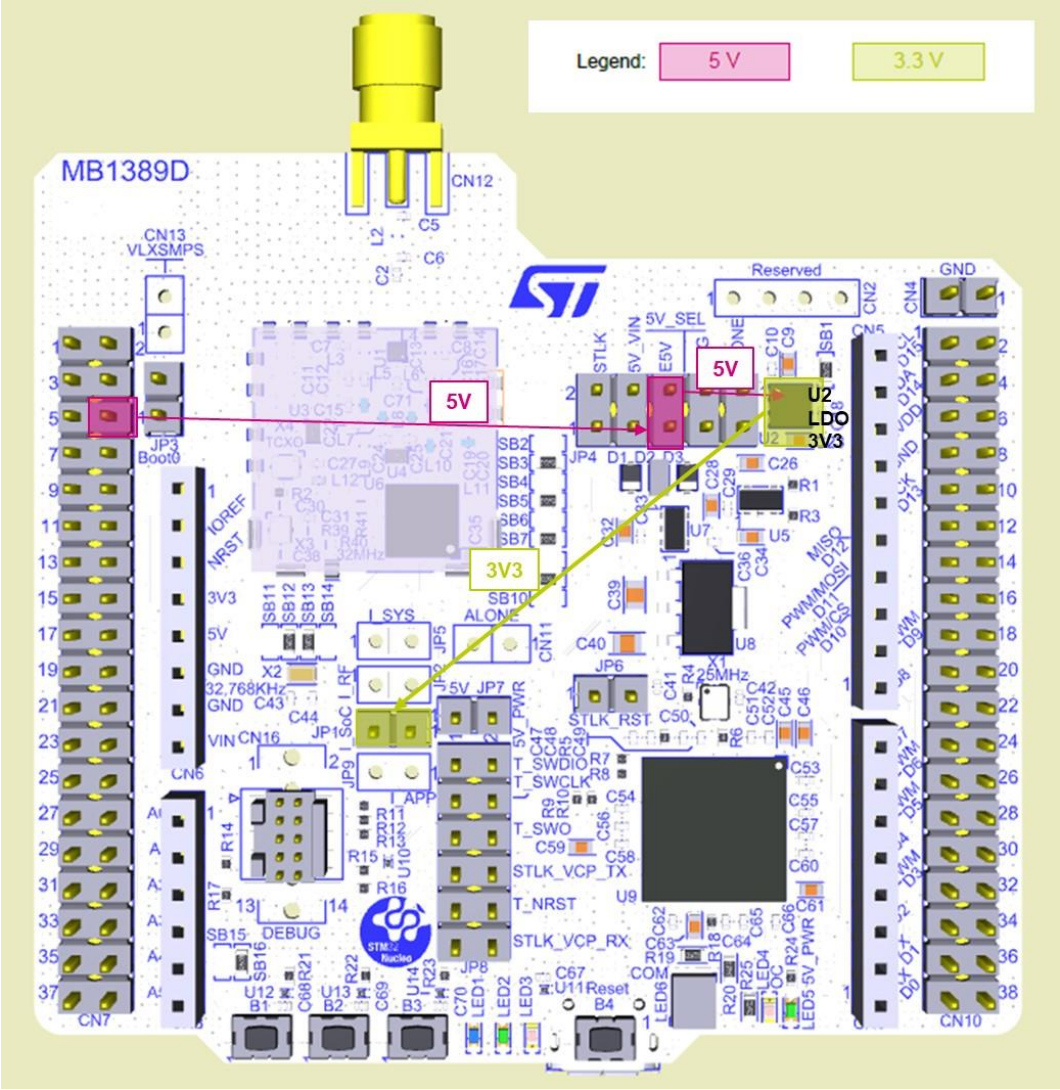
When the Nucleo-64 board is power-supplied by E5V (refer to Table 7 and Figure 13), the jumper configuration must be the following: JP4 [5-6] on E5V.

Table 7. External power sources: E5V (5 V)

Input power name	Connector pins	Voltage range	Maximum current
E5V	CN7 pin 6	4.75 to 5.25 V	500 mA

Refer to Section 6.4.1 for debugging when using an external power supply.

Figure 13. Power supply input from 5V_EXT (5 V, 500 mA maximum)



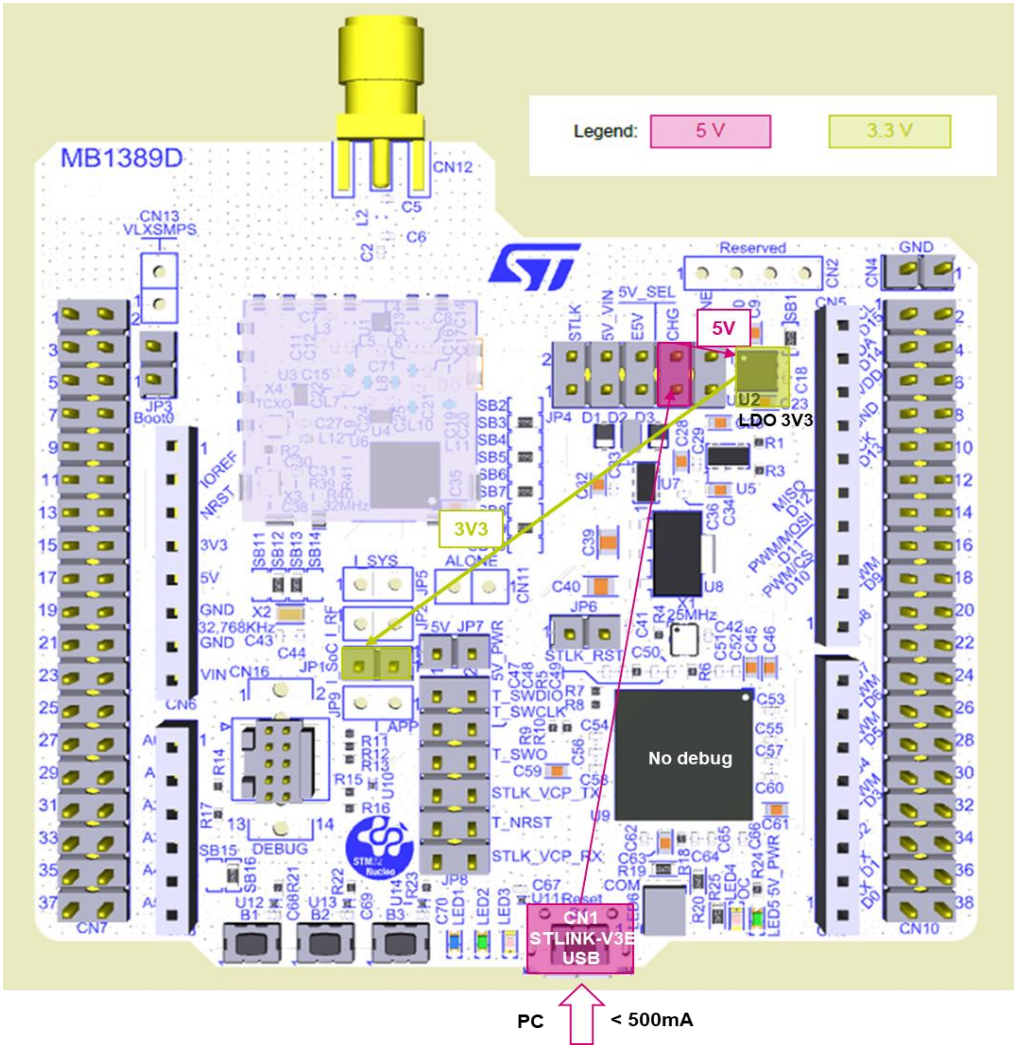
External power supply input from 5 V USB charger

When the Nucleo-64 board is power-supplied by a USB charger on CN1 (Refer to Table 8 and Figure 14), the jumper configuration must be the following: jumper JP4 [7-8] on 5V_CHGR.

Table 8. External power sources: 5V_CHGR (5 V)

Input power name	Connector pins	Voltage range	Maximum current
5V_CHGR	CN1	5 V	-

Figure 14. Power supply input from ST-LINK USB connector with 5 V USB charger

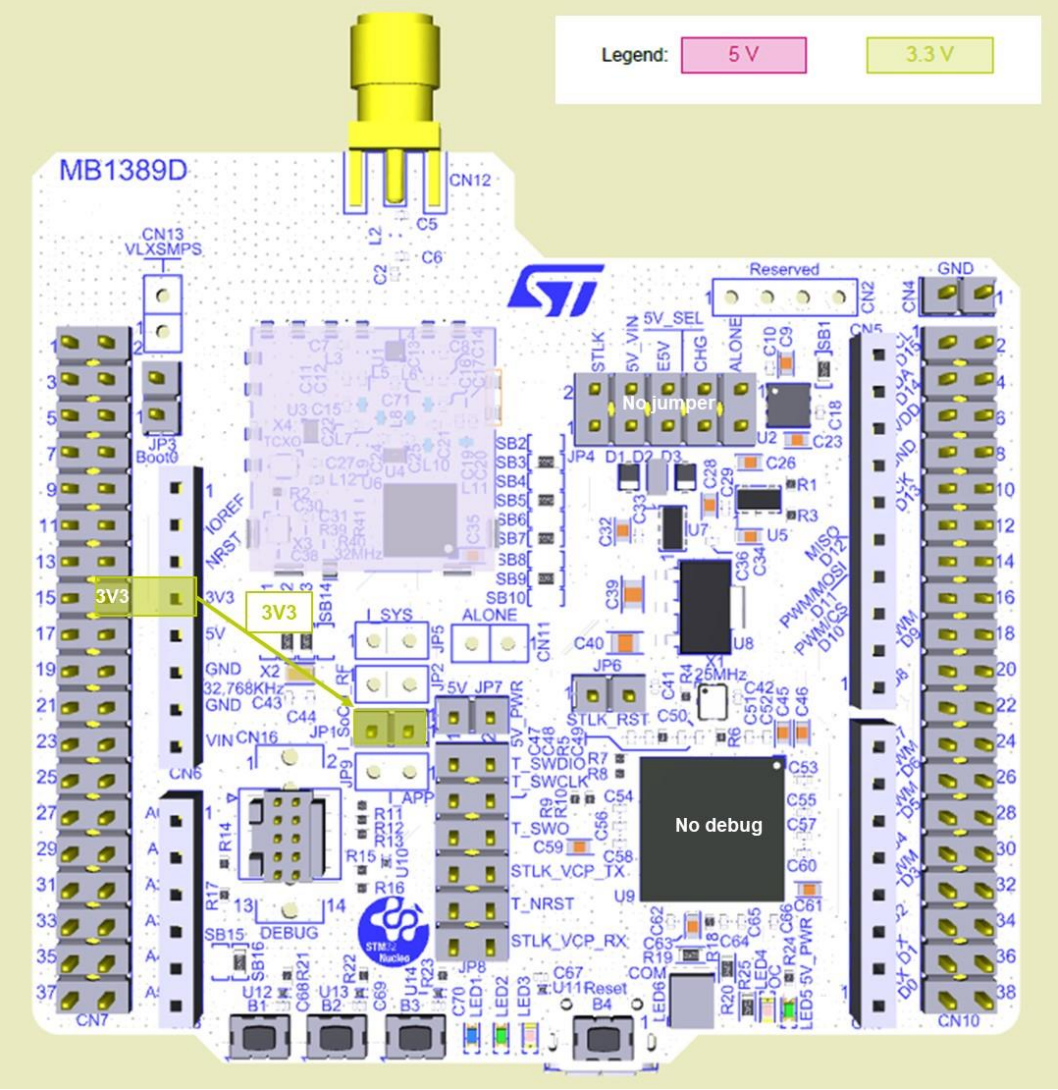


External power supply input from external 3.3 V

When the 3.3 V is provided by a shield board, it is interesting to use the 3.3 V (CN6 pin 4 or CN7 pin 16) directly as power input (refer to Table 9 and Figure 15). In this case, the programming and debugging features are not available, since the ST-LINK is not powered.

Table 9. External power sources: 3V3

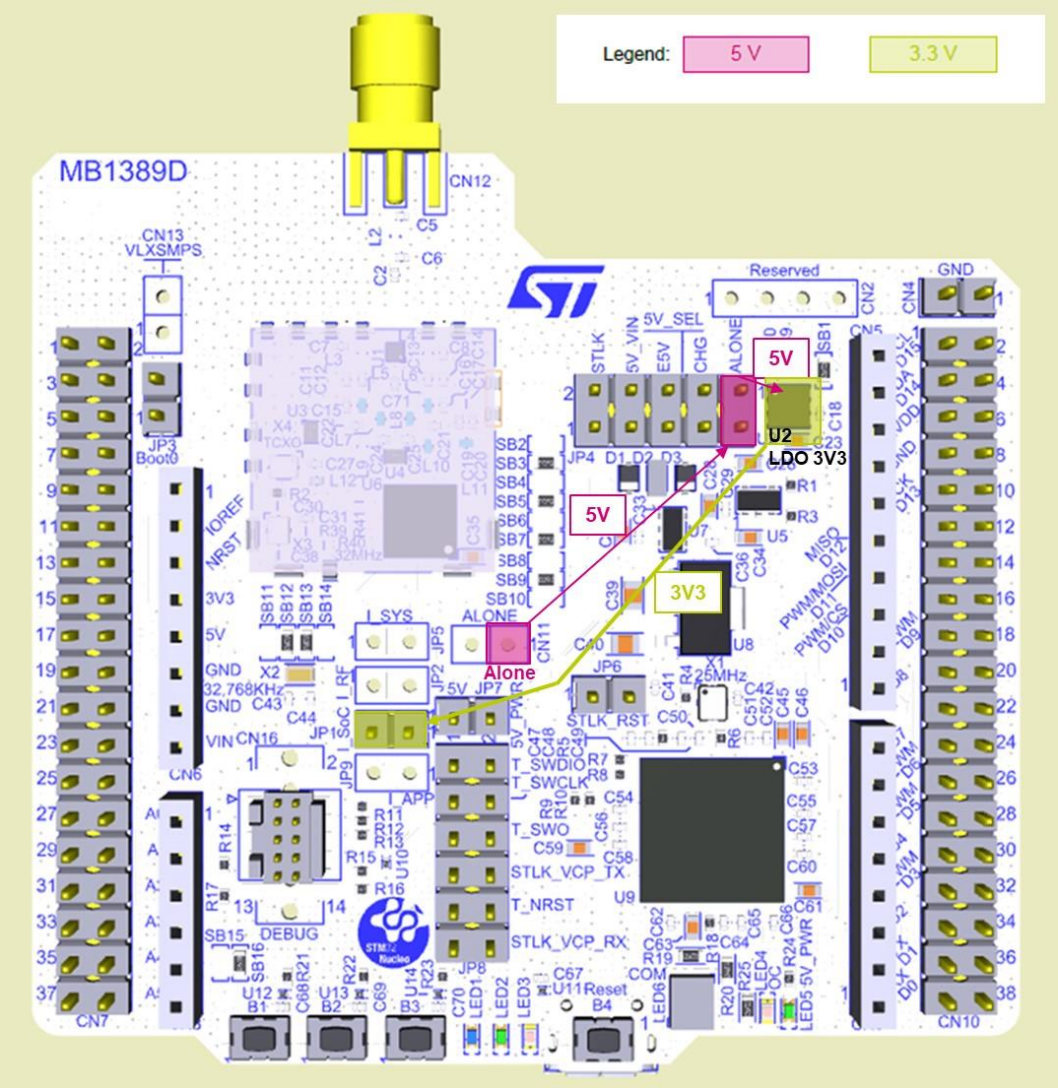
Input power name	Connector pins	Voltage range	Maximum current
3V3	CN6 pin 4 CN7 pin 16	3 to 3.6 V	1.3 A



External power supply input STD_ALONE_5V (5 V, 500 mA maximum)

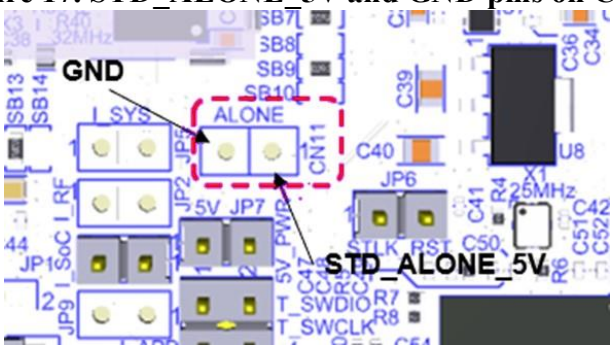
When the Nucleo-64 board is power-supplied by STD_ALONE_5V (refer to Table 10 and Figure 16), the jumper configuration must be the following: Jumper JP4 [9-10] on ALONE.

Figure 16. Power supply input from STD_ALONE_5V (5 V, 500 mA maximum)



When the board is supplied with STD_ALONE_5V (on connector 11), then the STLINK-V3E debugger is not supplied. Take care to correctly supply the board when using CN11. CN11 pin 1 is the STD_ALONE_5V supply and pin 2 is the GND, as shown in Figure 17.

Figure 17. STD_ALONE_5V and GND pins on CN11



To properly isolate the MCU STM32 WL from the STLINK-V3E debugger, it is recommended to remove the following jumpers: the 6 jumpers of JP8 and the jumper of JP7. In this case, there is no current leakage coming from the STLINK-V3E debugger in current consumptions.

5.4.1 Debugging while using VIN or EXT as an external power supply

When powered by VIN or E5V, it is still possible to use the ST-LINK for programming or debugging, but it is mandatory to power the board first using VIN or EXT, then to connect the USB cable to the PC. In this way, the enumeration succeeds, thanks to the external power source. The following power-sequence procedure must be respected:

1. Connect jumper JP4 between pins 5 and 6 for E5V or between pins 3 and 4 for VIN.
2. Connect the external power source to VIN or E5V.
3. Power on the external power supply 7 V < VIN < 12 V for VIN, or 5 V for E5V.
4. Check that the LED5 green LED is turned ON.
5. Connect the PC to the CN1 USB connector.

If this order is not respected, the board may be powered by USB first, then by VIN or E5V as the following risks may be encountered:

1. If more than 300 mA current is needed by the board, the PC may be damaged or the current supplied can be limited by the PC. As a consequence, the board is not powered correctly.
2. 300 mA is requested at enumeration so there is a risk that the request is rejected and the enumeration does not succeed if the PC cannot provide such current. Consequently, the board is not power supplied and LED5 remains OFF.

5.5 Clock sources

5.5.1 HSE clock (high-speed external clock)

There are two ways to configure the pins corresponding to the high-speed external clock (HSE):

- **HSE on-board oscillator from X3 crystal**: For typical frequencies, capacitors, and resistors, refer to the STM32 microcontroller datasheet and the application note *Oscillator design guide for STM8AF/AL/S, STM32 MCUs and MPUs* (AN2867) for the oscillator design guide. The X3 crystal has the following characteristics: 32 MHz, 10 pF load capacitance, 10 ppm. It is recommended to use NDK_NX2016SA 32MHz EXS00ACS06465 manufactured by NDK. The configuration must be:

  - X3 crystal (and X4 TCXO) soldered.
  - No C30 and no C38 as those capacitors are integrated into the MCU.
  - SB20 OFF in order not to supply the TCXO.
  - C31 OFF in order not to have a 32 MHz signal coming from the TCXO.
  - R39 and R40 ON to connect the X3 crystal to the 55 MCU.

- **HSE on-board oscillator from X4 TCXO (Default configuration)**: The X4 TCXO has the following characteristics: 32MHz, 10pF load capacitance. It is recommended to use NT2016SF-32M-END5875A manufactured by NDK. The configuration must be:

  - X4 TCXO (and X3 crystal) soldered.
  - SB20 ON to supply the TCXO.
  - 10 pF C31 and 220 Ω R2 ON to have a 32 MHz signal coming from the TCXO.
  - R39 and R40 OFF to isolate the X3 crystal from the 55 MCU.
  -

Note: Whatever the configuration is (X3 crystal or X4 TCXO), both X3 crystal and X4 TCXO are assembled on the board to avoid to solder or desolder either X3 or X4 to choose between X3 crystal and X4 TCXO configuration.

5.5.2 LSE clock (low-speed external clock) – 32.768 kHz

There are three ways to configure the pins corresponding to the low-speed clock (LSE):

- **On-board oscillator (Default)**: X2 crystal. Refer to the application note *Oscillator design guide for STM8AF/AL/S, STM32 MCUs and MPUs* (AN2867) as the oscillator design guide for STM32 microcontrollers. It is recommended to use NX3215SA-32.768kHz-EXS00A-MU00527 (32.768 kHz, 6 pF load capacitance, 20 ppm) from NDK.

  - SB11 and SB14 OFF
  - SB12 and SB13 ON

- **Oscillator from external PC14**: from external oscillator through the pin 25 of CN7 connector. The configuration must be:
  - SB11 (and SB14 ON, but not necessary)
  - SB12 and SB13 OFF

- **LSE not used**: PC14 and PC15 are used as GPIOs instead of the low-speed clock. The configuration must be:

  - SB11 and SB14 ON (to get them on CN7)
  - SB12 and SB13 OFF

5.6 Board functions

5.6.1 LEDs

LED1 user LED

This blue LED is a user LED connected to I/O PB15. To light the LED LED1, a HIGH logic state must be written in the corresponding GPIO PB15.

LED2 user LED

This green LED is a user LED connected to I/O PB9. To light the LED LED2, a HIGH logic state must be written in the corresponding GPIO PB9.

LED3 user LED

This red LED is a user LED connected to I/O PB11. To light the LED LED3, a HIGH logic state must be written in the corresponding GPIO PB11.

LED4 USB power fault (OC, overcurrent)

LED4 indicates that the board power consumption on USB ST-LINK exceeds 500 mA, consequently, the user must check the root cause of the overconsumption or power the board using an external power supply.

LED5 (5V_PWR)

The green LED indicates that the part is powered and +5 V power is available on CN6 pin 5 and CN7 pin 18 if the jumper JP7 is ON.

LED6 (STLINK-V3 COM LED)

The bicolor LED LED6 (green, red) provides information about STLINK-V3E communication status. LED6 indicates the communication progress between the PC and the STLINK-V3E, with the following setup:

- Blinking red: the first USB enumeration with the PC is taking place
- Red LED ON: when the initialization between the PC and STLINK-V3E is complete
- Blinking red or green: during programming and debugging with target
- Green LED ON: communication finished and successful
- Orange ON: communication failure

5.6.2 Push-buttons

B1 (USER)

The user button is connected to the I/O PA0 by default (WKUP1, SB16 ON, and SB15 OFF) or PC13 (WKUP2, SB15 ON, and SB16 OFF) of the microcontroller.

B2 (USER)

The user button is connected to the I/O PA1 of the microcontroller.

B3 (USER)

The user button is connected to the I/O PC6 of the microcontroller.

B4 (RESET)

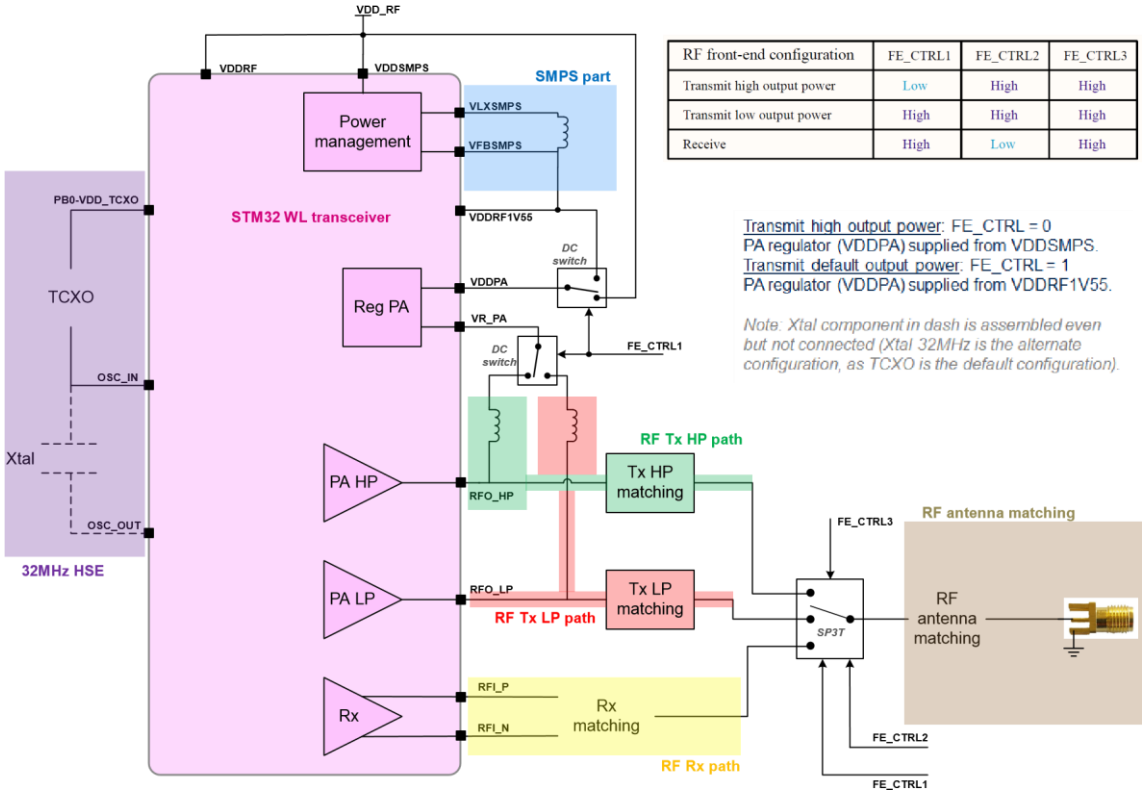
This push-button is connected to NRST and is used to RESET the microcontroller.

5.6.3 RF overview

The Nucleo-64 board embeds an RF 3-port switch (SP3T) to address, with the same board the three modes: reception, high-power transmission, and low-power transmission. The choice between the two transmission modes can be done dynamically, thanks to two DC switches controlled by FE_CTRL1 (GPIO from MCU):

- The transmission high-output power amplifier (PA HP) is supplied from the PA regulator (REG PA) up to 3.1 V. For this, the REG PA must be supplied directly from VDDSMPS.
- The transmission default low-output power amplifier (PA LP) can be supplied from the PA regulator (REG PA) up to 1.35 V. For this, the REG PA must be supplied from the regulated VFBSMPS supply at 1.55 V.

The RF block diagram is displayed in Figure 18.



RF front-end configuration	FE_CTRL1	FE_CTRL2	FE_CTRL3
Transmit high output power	Low	High	High
Transmit low output power	High	High	High
Receive	High	Low	High

Transmit high output power: FE_CTRL = 0
PA regulator (VDDPA) supplied from VDDSMPS.
Transmit default output power: FE_CTRL = 1
PA regulator (VDDPA) supplied from VDDRF1V55.

Note: Xtal component in dash is assembled even but not connected (Xtal 32MHz is the alternate configuration, as TCXO is the default configuration).

The screwed and glue-fixed antennas to connect on the SMA connector and provided in the blister are:

- ANT-SS900 from LPRS company for NUCLEO-WL55JC1 (high band frequency)
- ANT-SS450-510 from LPRS company for NUCLEO-WL55JC2 (low band frequency)

Those antennas have been used for the different FCC/ISED/CE certifications. It is then mandatory to use those referenced antennas (and only those) for radiated tests on the Nucleo-64 boards.

The antenna is stuck to the SMA connector because of FCC constraints. Indeed, it is mentioned for the FCC regulations, that as soon as a product is considered general public, the FCC implies that the antenna must be stuck to the board connector with epoxy glue. Refer to the FCC documentation BASIC EQUIPMENT AUTHORIZATION .

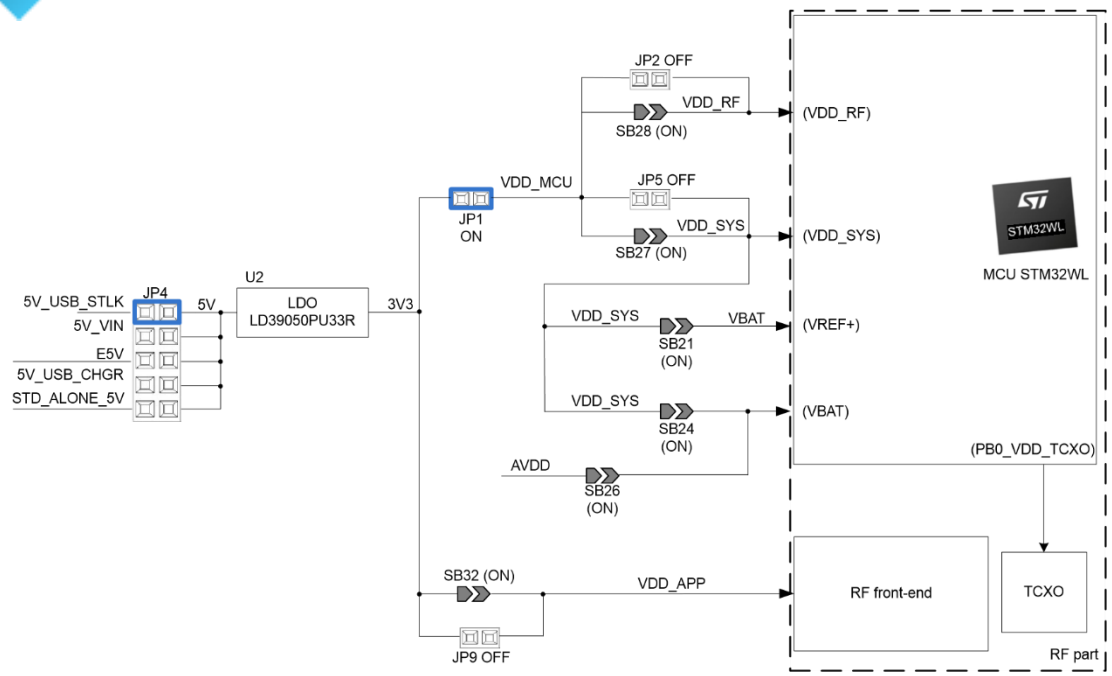
GUIDANCE FOR ANTENNAS USED WITH PART 15 INTENTIONAL RADIATORS in the chapter ANTENNA REQUIREMENTS—Section 15.203. The purpose of Section 15.203 is to prevent attaching any other antenna(s) [other than one(s) approved with the device] to a Part 15 transmitter.

5.6.4 Current consumption measurement (I_SoC)

Jumper JP1, labeled I_SoC, is used to measure the microcontroller consumption by removing the jumper and by connecting an ammeter. Their location in the power structure is shown in Figure 19.

1. JP1 ON. is powered with 3V3 voltage (default)
2. JP4 OFF. An ammeter must be connected to measure the current. If there is no ammeter, the STM32 is not powered.

Figure 19. JP1 and JP4 settings for current consumption measurement



Note:

I_SoC (on VDD_MCU) is the current consumption of all the MCU.

I_RF (on VDD_RF) is the current consumption of the RF part of the MCU.

I_SYS (on VDD_SYS) is the current consumption of the rest of the MCU (except I-RF).

So I_SoC = I_RF + I_SYS

We can evaluate the current consumption of the RF part of the MCU by connecting an ammeter on JP2. SB28 must be OFF in this case.

We can also evaluate the current consumption of the rest of the MCU (VDD_SYS) by connecting an ammeter on JP5. SB27 must be OFF in this case.

We can also evaluate the RF front-end current consumption (VDD_APP) by connecting an ammeter on JP9. SB32 must be OFF in this case. This current consumption only concerns both NX3L1T3157GM DC switches (U3 and U4).

5.6.5 Virtual COM port (VCP): LPUART and USART

The Nucleo-64 board offers the possibility to select which USART interface is connected to the STLINK-V3E, Uno V3 connector (CN9 pins 2 and 1), or to the ST morpho connector (CN10 pins 35 and 37).

The selection is done by setting the related solder bridges as detailed in Table 11 and Table 12.

Table 11. USART1 connection

Solder bridge configuration(1)	Feature(1)
SB6, SB10: ON SB7, SB9, SB3, SB5: OFF	USART1 (PB6/PB7) connected to STLINK-V3E virtual COM port.
SB7, SB9: ON	USART1 (PB6/PB7) connected to Arduino™ (D1 & D0) and ST morpho connector (CN10 pin 35 and 37).

1. The default configuration is shown in bold

Solder bridge configuration(1)	Feature(1)
SB3, SB5: ON SB2, SB4, SB6, SB10: OFF	LPUART1 (PA2/PA3) connected to STLINK-V3E Virtual COM port.
SB2, SB4: ON SB3, SB5, SB7, SB9: OFF	LPUART1 (PA2/PA3) connected to (D1 & D0) and ST morpho connector (CN10 pin 35 and 37).

Table 12. LPUART1 connection

Solder bridge configuration(1)			Feature(1)
SB6, SB10, SB2, SB4: OFF			
3.3 V LDO output	SB1	ON	U2 LDO output provides 3.3 V
		OFF	U2 LDO output does NOT provide 3.3 V. The user must connect an external 3V3 source.
PA2 LPUART1 TX	SB2	ON	ARD_D1_TX connected to LPUART1 TX PA2
		OFF	ARD_D1_TX not connected to LPUART1 TX PA2
	SB3	ON	STLINK_TX (T_VCP_TX) connected to LPUART1 TX PA2
		OFF	STLINK_TX (T_VCP_TX) not connected to LPUART1 TX PA2
PA3 LPUART1 RX	SB4	ON	ARD_D0_RX connected to LPUART1 RX PA3
		OFF	ARD_D0_RX not connected to LPUART1 RX PA3
	SB5	ON	STLINK_RX (T_VCP_RX) connected to LPUART1 RX PA3
		OFF	STLINK_RX (T_VCP_RX) not connected to LPUART1 RX PA3
PB6 USART1 TX	SB6	ON	STLINK_TX (T_VCP_TX) connected to USART1 TX PB6
		OFF	STLINK_TX (T_VCP_TX) not connected to USART1 TX PB6
	SB7	ON	ARD_D1_TX connected to USART1 TX PB6
		OFF	ARD_D1_TX not connected to USART1 TX PB6
T_SWO on PB3	SB8	ON	T_SWO connected to PB3

By default:

- Communication between the target and the STLINK-V3E MCU is enabled on LPUART1 to support the Virtual COM port.
- Communication between the target and (and ST morpho) connectors is enabled on USART1.

5.7 Solder bridges

All the 31 solder bridges are located on the Nucleo-64 board.

All the solder bridges present on the Nucleo-64 board are used to configure several I/Os and power supply pins for compatibility of features and pinout with the target supported.

Table 13. Solder bridge configuration

Solder bridge control	Solder bridge (SB)	State (1)	Description (1)
T_SWO on PB3	SB8	OFF	T_SWO not connected to PB3 and isolated from ARD_D3
PB7 USART1 RX	SB9	ON	ARD_D0_RX connected to USART1 RX PB7
		OFF	ARD_D0_RX not connected to USART1 RX PB7
	SB10	ON	STLINK_RX (T_VCP_RX) connected to USART1 RX PB7
		OFF	STLINK_RX (T_VCP_RX) not connected to USART1 RX PB7
LSE CLK selection	SB11	ON	PC14-OSC32_IN connected to ST morpho connector I/O usage (CN7 pin 25)
		OFF	PC14-OSC32_IN not connected to ST morpho connector
	SB12 / SB13	ON	LSE provided by external LSE 32.768kHz CLK X2
		OFF	LSE not provided by external LSE 32.768kHz CLK X2
	SB14	ON	PC15-OSC32_OUT connected to ST morpho connector I/O usage (CN7 pin 27)
		OFF	PC15-OSC32_OUT not connected to ST morpho connector
B1 User button	SB15	ON	User button connected to PC13

		OFF	User button not connected to PC13
	SB16	ON	User button connected to PA0
		OFF	User button not connected to PA0
SP3T VDD supply	SB18	ON	VDD supplied with FE_CTRL3 (IO PC3)
		OFF	VDD not connected to FE_CTRL3 (IO PC3)
BOOT0/PH3 on STmorpho connector	SB19	ON	BOOT0/PH3 connected to ST Morpho connector CN7 pin 7
		OFF	BOOT0/PH3 not connected to ST Morpho connector CN7 pin 7
32 MHz TCXO supply	SB20	ON	32 MHz TCXO supplied by PB0-VDD_TCXO (to)
		OFF	32 MHz TCXO disconnected to PB0-VDD_TCXO (to)
VBAT	SB21	ON	VBAT (pin A8 of) powered by VDD_SYS
		OFF	VBAT (pin A8 of) supplied separately (through VBAT on ST morpho connector CN7 pin 33)
VFBSMPS	SB22	ON	VFBSMPS (pin B2 of) connected to VDDRF1V55 (pin F7 of)
		OFF	VFBSMPS (pin B2 of) disconnected from VDDRF1V55 (pin F7 of) for current probing
VDDSMPS	SB23	ON	VDDSMPS (pin A2 of) connected to VDDRF (pin E8 of)
		OFF	VDDSMPS (pin A2 of) disconnected from VDDRF (pin E8 of) for current probing
VDDA / VREF+ supply	SB24	ON	VDDA/VREF+ supplied by VDD_SYS through SMD ferrite bead L14. Be careful not to provide an external AVDD supply if SB26 is ON.
		OFF	VDDA/VREF+ disconnected from VDD_SYS. VDDA/VREF+ must be externally supplied by AVDD.
IOREF and 3V3 connection	SB25	ON	IOREF connected to the 3V3 power supply. Be careful to remove SB29 to avoid voltage supply conflict with VDD_MCU.
Solder bridge control	Solder bridge (SB)	State(1)	Description(1)

IOREF and 3V3 connection	SB25	OFF	IOREF not connected to 3V3 power supply
VDDA / VREF+ supply	SB26	ON	VDDA/VREF+ externally supplied by AVDD. SB24 must be OFF to avoid supply conflict.
		OFF	VDDA/VREF+ disconnected from AVDD. So SB24 must be ON to supply properly VDDA/VREF+ pins.
I_SYS current probing	SB27	ON	VDD_SYS generated from VDD_MCU
		OFF	For I_SYS current probing on JP5 jumper
I_RF current probing	SB28	ON	VDD_RF generated from VDD_MCU
		OFF	For I_RF current probing on JP2 jumper
IOREF and VDD_MCU connection	SB29	ON	IOREF connected to the VDD_MCU power supply. Be careful to remove SB25 to avoid voltage supply conflict with 3V3
		OFF	IOREF not connected to VDD_MCU power supply
PB0 on ST morpho connector	SB30	ON	PB0 connected to ST morpho connector (CN10 pin 22)
		OFF	PB0 not connected to ST morpho connector
PB3 on morpho	SB31	ON	PB3 connected to Arduino™ D3
		OFF	PB3 not connected to Arduino™ D3
I_APP current probing	SB32	ON	RF front-end supply VDD_APP generated from VDD_MCU
		OFF	For I_APP current probing on JP9 jumper

6. Board connectors

Several connectors are implemented on the Nucleo-64 board.

6.1 CN1 STLINK-V3E USB Micro-B connector

The CN1 USB Micro-B connector is used to connect the embedded STLINK-V3E to a PC for programming and debugging purposes.

Figure 20. USB Micro-B connector CN23 (front view)

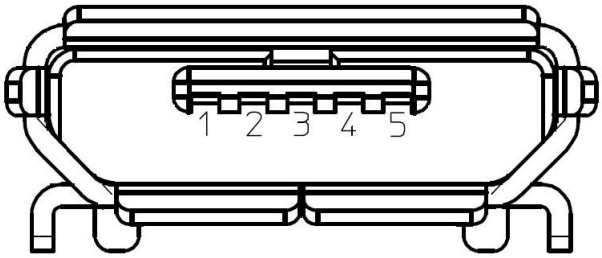
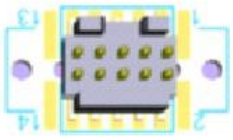


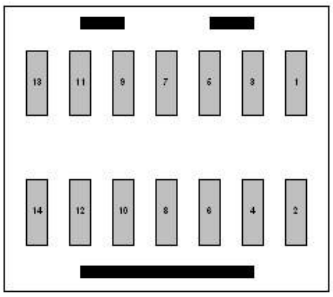
Table 14. USB Micro-B connector CN23 (front view)

Connector	Pin number	Pin name	Signal name	STLINK-V3EMCU pin	Functions
CN1	1	VBUS	5V_USB_CHGR	-	5 V Power
	2	DM	USB_DEV_HS_CN_N	R14	USB differential pair N
	3	DP	USB_DEV_HS_CN_P	R15	USB differential pair P
	4	ID	-	-	-
	5	GND	-	-	GND

6.2 CN16 MIPI10 connector

Figure 21. MIPI10 debugging connector CN16 (top view)





The connector is implemented with a footprint compatible with the STDC14 footprint. The related pinout for the MIPI10 connector is listed in Table 15.

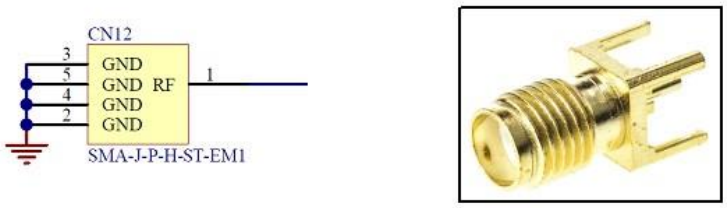
Table 15. CN16 MIPI10 connector pinout (STDC14 pinout compatible)

Connector	Pin number	Description	Pin number	Description
CN16	1	-	2	-
	3	VDD (3V3)	4	T_SWDIO (PA13)
	5	GND	6	T_SWCLK (PA14)
	7	KEY (connected to GND)	8	T_SWO (PB3)
	9	-	10	T_JTDI (PA15)
	11	GNDDetect (connected to GND through a 100 Ω resistor)	12	T_NRST
	13	T_VCP_RX (PA3 by default or PB7)	14	T_VCP_TX (PA2 by default or PB6)

6.3 CN12 SMA connector

CN12 50 Ω SMA connector is available on the Nucleo-64 board.

Figure 22. CN12 SMA connector



By default, the output of the RF part is on the CN12 SMA connector.

Table 16. SMA connector pinout

Connector	Pin number	Description
CN12	1	RF path
	2	GND
	3	GND
	4	GND
	5	GND

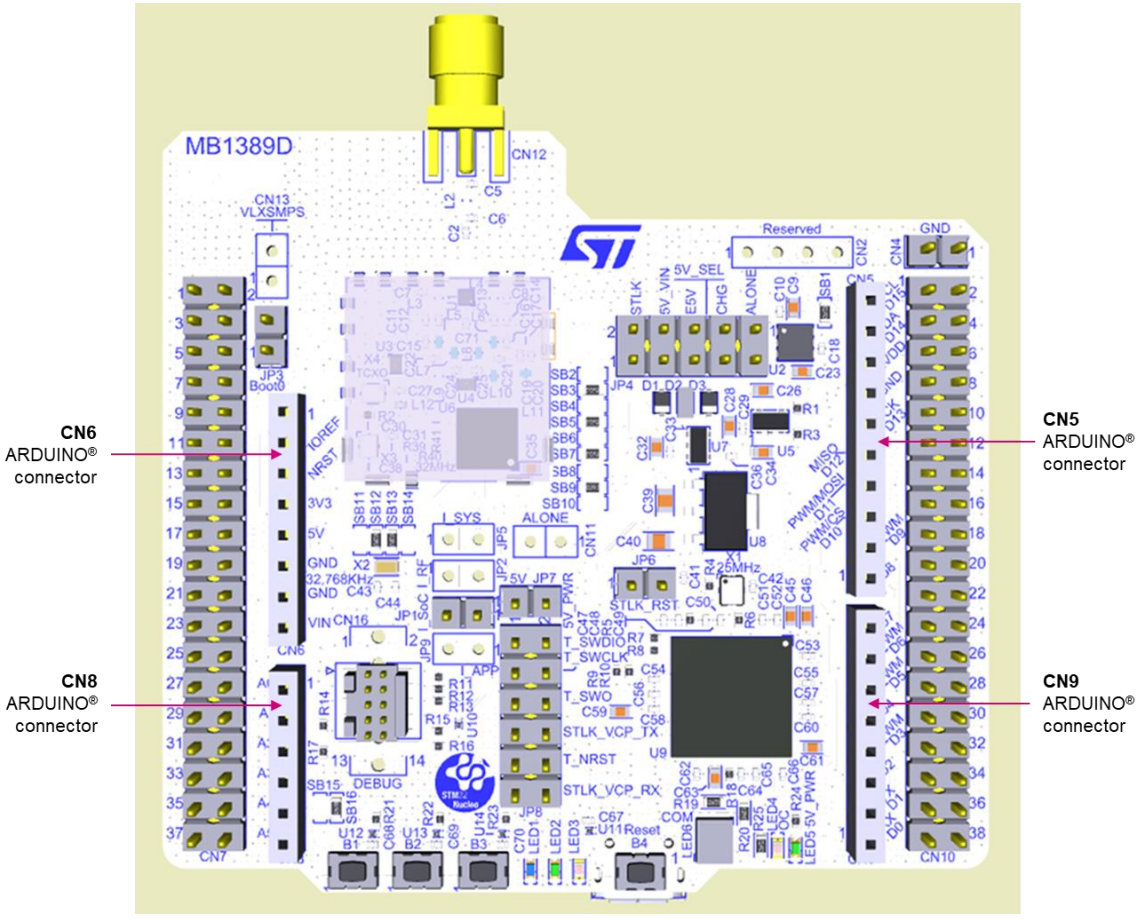
CN5, CN6, CN8, and CN9: Uno V3 connector

6.4 CN5, CN6, CN8, and CN9: Uno V3 connector

CN5, CN6, CN8, and CN9 are female connectors compatible with the standard. Refer to Figure 23 for their location. Most shields designed for can fit with the Nucleo-64 board.

The connector on the Nucleo-64 board supports the Uno V3.

Figure 23. connector



The related pinout for the connector is listed in Table 17.

Note: Uno V3 D0 and D1 signals are connected by default on USART1 (MCU I/O PB6 and PB7). Refer to Section 6.6.5 for details on how to modify the UART interface.

Table 17. connector pinout

Connector	Pin number	Pin name	Signal name	STM32 pin (1)	Function (1)
CN6	1	NC	-	-	Reserved for test
	2	IOREF	-	-	I/O reference
	3	NRST	T_NRST	NRST	RESET
	4	3V3	-	-	3.3 V input/output
	5	5V	-	-	5 V output
	6	GND	-	-	GND

CN5, CN6, CN8, and CN9: Uno V3 connector

Connector	Pin number	Pin name	Signal name	STM32 pin(1)	Function(1)
CN6	7	GND	-	-	GND
	8	VIN	-	-	7 V - 12 V input power
CN8	1	A0	ADC	PB1	ADC1_IN5
	2	A1	ADC	PB2	ADC1_IN4
	3	A2	ADC	PA10	ADC1_IN6
	4	A3	ADC	PB4	ADC1_IN3
	5	A4	ADC	PB14	ADC1_IN1 / I2C3_SDA
	6	A5	ADC	PB13	ADC1_IN0 / I2C3_SCL
CN5	1	D8	ARD_D8	PC2	IO
	2	PWM / D9	ARD_D9	PA9	TIM1_CH2
	3	PWM /CS / D10	ARD_D10	PA4	LPTIM1_OUT / SPI1_NSS

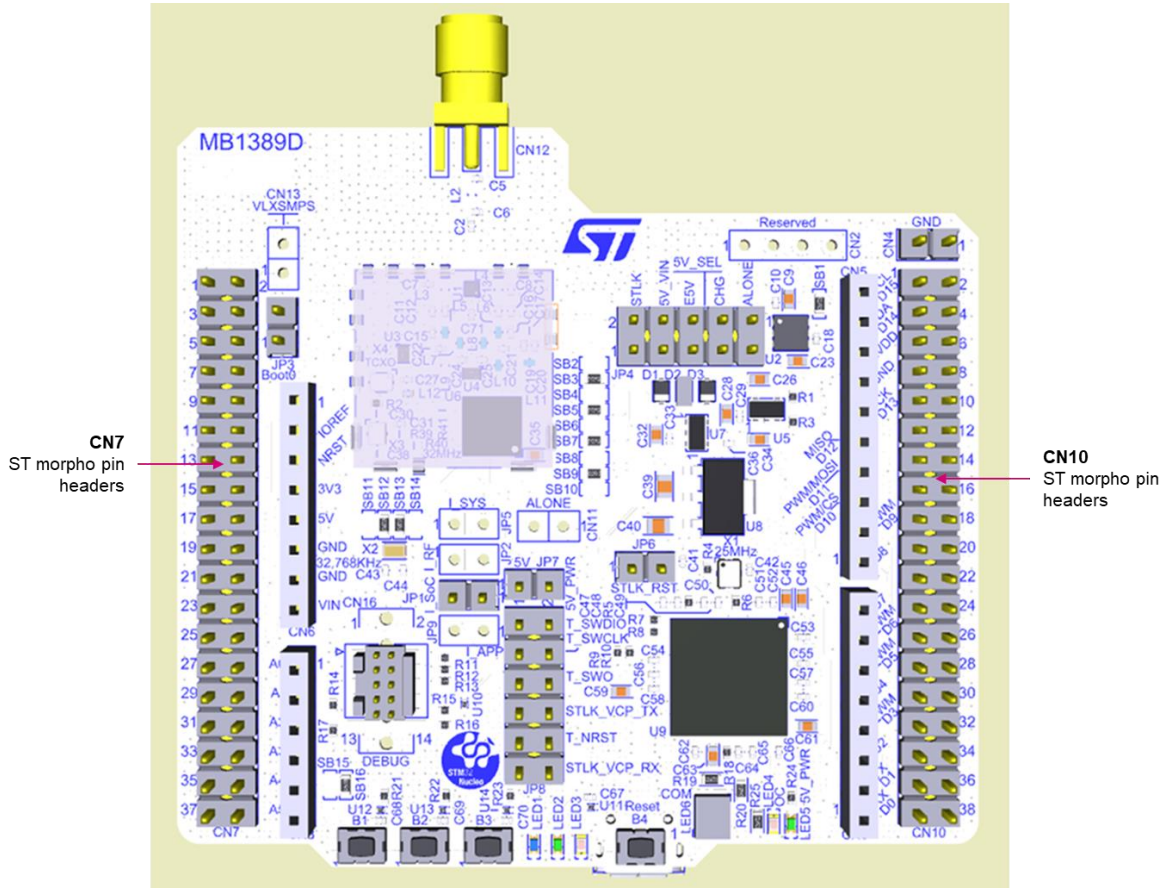
	4	PWM / MOSI / D11	ARD_D11	PA7	TIM17_CH1 / SPI1_MOSI
	5	MISO / D12	ARD_D12	PA6	SPI1_MISO
	6	SCK / D13	ARD_D13	PA5	SPI1_SCK
	7	GND	-	-	GND
	8	AVDD	AVDD	AVVD / VREF+	Voltage reference
	9	SDA / D14	ARD_D14	PA11	I2C2_SDA
	10	SCL / D15	ARD_D15	PA12	I2C2_SCL
CN9	8	D7	ARD_D7	PC1	IO
	7	PWM / D6	ARD_D6	PB10	TIM2_CH3
	6	PWM/D5	ARD_D5	PB8	TIM16_CH1
	5	D4	ARD_D4	PB5	IO
	4	PWM / D3	ARD_D3	PB3	TIM2_CH2
	3	D2	ARD_D2	PB12	IO
	2	TX / D1	ARD_D1	PA2 / PB6	LPUSART1_TX / USART1_TX
	1	RX / D0	ARD_D0	PA3 / PB7	LPUSART1_RX / USART1_RX

1.Default configuration is in bold.

6.5 CN7 and CN10 ST morpho connectors

CN7 and CN10 ST morpho connectors are male pin headers accessible on both sides of the board. All signals and power pins of the MCU are available on the morpho connectors. These connectors can also be probed by an oscilloscope, logical analyzer, or voltmeter.

Figure 24. ST morpho connectors



Note: The D0 and D1 signals are connected by default to USART1 (MCU I/O PB6 and PB7). Refer to Section 6.6.5 for details about how to modify the UART interface. Table 18 shows the pin assignment of each I/O on the ST morpho connector.

Table 18. Pin assignment of the ST morpho connectors

CN7 odd pins		CN7 even pins		CN10 odd pins		CN10 even pins	
Pin nbr	Pin name	Pin nbr	Pin name(1)	Pin nbr	Pin name(1)	Pin nbr	Pin name
1	NC	2	NC	1	PA0	2	PC4
3	NC	4	NC	3	PA12	4	PC5
5	VDD_MCU	6	E5V	5	PA11	6	NC
7	BOOT0	8	GND	7	AVDD	8	5V_USB_CHGR(2)
9	NC	10	NC	9	GND	10	NC
11	NC	12	IOREF	11	PA5	12	PC6

CN7 and CN10 ST morpho connectors

CN7 odd pins		CN7 even pins		CN10 odd pins		CN10 even pins	
Pin nbr	**Pin name**	**Pin nbr**	**Pin name(1)**	**Pin nbr**	**Pin name(1)**	**Pin nbr**	**Pin name**
13	PA13(3)	14	NRST	13	PA6	14	PC0
15	PA14(3)	16	3V3	15	PA7	16	PA8
17	PA15	18	5V	17	PA4	18	NC
19	GND	20	GND	19	PA9	20	GND
21	NC	22	GND	21	PC2	22	PB0
23	PC13	24	VIN	23	PC1	24	NC
25	PC14	26	NC	25	PB10	26	PB9
27	PC15	28	PB1	27	PB8	28	PB15
29	NC	30	PB2	29	PB5	30	PB11
31	NC	32	PA10	31	PB3	32	AGND
33	VBAT	34	PB4	33	PB12	34	NC
35	NC	36	PB14	35	PB6 / PA2	36	PA1
37	NC	38	PB13	37	PB6 / PA3	38	PC3

1. Default configuration in bold.
2. 5V_USB_CHGR is the 5 V power from the STLINK-V3E USB connector that rises first. It rises before the 5 V rising on the board.

3. PA13 and PA14 are shared with SWD signals connected to STLINK-V3E. It is not recommended to use them as I/O pins.

7. NUCLEO-WL55JC board information

7.1 Product marking

The stickers located on the top or bottom side of the PCB provide product information:

- Product order code and product identification for the first sticker.
- Board reference with revision, and serial number for the second sticker.

On the first sticker, the first line provides the product order code, and the second line the product identification.

On the second sticker, the first line has the following format: “MBxxxx-Variant-yzz”, where “MBxxxx” is the board reference, “Variant” (optional) identifies the mounting variant when several exist, "y" is the PCB revision and "zz" is the assembly revision, for example B01. The second line shows the board serial number used for traceability.

Evaluation tools marked as “ES” or “E” are not yet qualified and therefore not ready to be used as reference design or in production. Any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering sample tools as reference designs or in production.

“E” or “ES” marking examples of location:

- On the targeted STM32 that is soldered on the board
- Next to the evaluation tool ordering part number that is stuck or silk-screen printed on the board.

Some boards feature a specific STM32 device version, which allows the operation of any bundled commercial stack/library available. This STM32 device shows a "U" marking option at the end of the standard part number and is not available for sales.

In order to use the same commercial stack in his application, a developer may need to purchase a part number specific to this stack/library. The price of those part numbers includes the stack/library royalties.

7.2 Product history

7.2.1 Product identification NUWL55JC1$XXX

This product identification is based on the MB1389-HIGHBAND-D04 board. It embeds the 55JC module with revision code "1". The limitations of this revision are detailed in the errata sheet 55xx, 54xx device errata (ES0500).

Product limitations

No limitation identified for this product identification.

7.2.2 Product identification NUWL55JC1$YYY

This product identification is based on the MB1389-HIGHBAND-E02 board. It embeds the 55JC module with revision code "2". The limitations of this revision are detailed in the errata sheet 55xx, 54xx device errata (ES0500).

Product limitations

No limitation identified for this product identification.

7.3 Board revision history

7.3.1 Board revision D04

The revision D04 is the initial release of the board.

7.3.2 Board revision E02

The revision E02 of the board is the final version with the updated MCU revision. In addition, the layout includes 8 more decoupling capacitors on voltages supplies to better filter the noise at its voltage's supplies.

7.3.3 Board limitations

The maximum output power is limited to 19.7 dBm to fulfill FCC/IC/CE requirements. An output power higher than 19.7 dBm at the antenna is prohibited.

Appendix A Nucleo-64 I/O assignment

Table 19. Nucleo-64 I/O assignment

Pin	Pin name	Signal or label	Main feature / optional feature / (SB)(1)
A1	VSSSMPS	VSSSMPS	GND of LDO/SMPS step-down converter
A2	VDDSMPS	VDDSMPS	External power supply of LDO/SMPS step-down converter
A4	PA14	T_SWCLK	T_SWCLK
A5	VDDA	VDDA	Analog voltage supply
A7	VDD	VDD	VDD voltage supply
A8	VBAT	VBAT	VBAT voltage supply
A9	PA12	PA12	ARD_D15 - I2C2_SCL
B1	VLXSMPS	VLXSMPS	VLXSMPS pin of SMPS step-down converter
B2	VFBSMPS	VFBSMPS	1.55 V provided by the SMPS step-down converter
B3	PA15	T_JTDI	T_JTDI
B4	PB15	PB15	LED1
B5	VREF+	VREF+	Input reference voltage for ADC
B6	PC14-OSC32_IN	OSC32_IN / PC14	**LSE_CLK** / GPIO PC14
B7	VSS	GND	GND
B8	PA13	T_SWDIO	T_SWDIO
B9	PA11	PA11	ARD_D14 - I2C2_SDA
C1	PB3	PB3	ARD_D3 - TIM2_CH2 / T_SWO
C2	PB4	PB4	ARD_A3 - ADC1_IN3
C3	PB7	LPUART1_RX	**ARD_D0** / STLINK_RX (T_VCP_RX)
C4	PB9	PB9	LED2
C5	PC15-OSC32_OUT	OSC32_OUT / PC15	**LSE CLK** / GPIO PC15
C6	PB14	PB14	ARD_A4 - ADC1_IN1/I2C3_SDA
C7	PC13	PC13	**GPIO PC13** / B1 user button
C8	PA10	PA10	ARD_A2 - ADC1_IN6
D2	PB5	PB5	ARD_D4 - IO
D3	PB8	PB8	ARD_D5 - TIM16_CH1
D4	PC2	PC2	ARD_D8 - IO
D5	PC3	PC3	FE_CTRL3
D6	PA0	PA0	B1 user button / GPIO PA0
D7	PB13	PB13	ARD_A5 - ADC1_IN0/I2C3_SCL

D8	PB2	PB2	ARD_A1 - ADC1_IN4
D9	VSS	GND	GND
E1	PB6	LPUART1_TX	**ARD_D1** / STLINK_TX (T_VCP_TX)
E2	VDD	VDD	VDD voltage supply
E3	VSS	GND	GND
E4	PC5	PC5	FE_CTRL2
E5	PA9	PA9	ARD_D9 - TIM1_CH2

Nucleo-64 I/O assignment

Pin	Pin name	Signal or label	Main feature / optional feature / (SB)[1]
E6	PB12	PB12	ARD_D2 - IO
E7	PB1	PB1	ARD_A0 - ADC1_IN5
E8	VDDRF	VDDRF	VDD supply for the RF part
E9	VDD	VDD	VDD voltage supply
F1	PC1	PC1	ARD_D7 - IO
F2	PC0	PC0	IO
F3	PC4	PC4	FE_CTRL1
F4	PA6	PA6	ARD_D12 - SPI1_MISO
F5	NRST	T_NRST	RESET
F6	PB0-VDD_TCXO	PB0-VDD_TCXO	**Supply voltage of TCXO** / GPIO PB0
F7	VDDRF1V55	VDDRF1V55	External power supply for the radio
F8	OSC_OUT	OSC_OUT	HSE CLK
G2	PC6	PC6	B3 user button
G3	PA1	PA1	B2 user button
G4	PB11	PB11	LED3
G5	VSS	GND	GND
G6	VSSRF	VSSRF	GND for RF part
G7	VSSRF	VSSRF	GND for RF part
G8	VSSRF	VSSRF	GND for RF part
G9	OSC_IN	OSC_IN	HSE CLK
H1	PA3	LPUART_RX	**STLINK RX (T VCP RX)** / ARD_D0
H2	PA2	LPUART_TX	**STLINK_TX (T_VCP_TX)** / ARD_D1

H3	PA7	PA7	ARD_D11 - TIM17_CH1/SPI1_MOSI
H4	PB10	PB10	ARD_D6 - TIM2_CH3
H5	VDD	VDD	VDD voltage supply
H6	VSSRF	VSSRF	GND for RF part
H7	RFI_N	RFI_N	RF receive input (differential N path)
H8	VDDPA	VDDPA	Input supply for PA regulator
H9	VR_PA	VR_PA	Regulated PA supply output
J1	PA4	PA4	ARD_D10 - LPTIM1_OUT/SPI1_NSS
J2	PA5	PA5	ARD_D13 - SPI1_SCK
J3	PA8	PA8	IO
J5	PH3	PH3	BOOT0
J6	RFI_P	RFI_P	RF receive input (differential P path)
J8	RFO_LP	RFO_LP	Transmit default power PA output
J9	RFO_HP	RFO_HP	Transmit high-power PA output

Appendix B Federal Communications Commission (FCC) and Innovation, Science and Economic Development Canada (ISED) Compliance Statements

B.1 FCC Compliance Statement

Part 15.19

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Part 15.21

Any changes or modifications to this equipment not expressly approved by STMicroelectronics may cause harmful interference and void the user's authority to operate this equipment.

Part 15.105

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instruction, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception which can be determined by turning the equipment off and on, the user is encouraged to try to correct interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Note: Use only shielded cables.

B.2 Additional FCC and ISED Compliance Statements

ISED License-Exempt Radios Apparatus

This device contains license-exempt transmitter(s)/receiver(s) that comply with Innovation, Science and Economic Development Canada's license-exempt RSS(s). Operation is subject to the following two conditions:

1. This device may not cause interference.
2. This device must accept any interference, including interference that may cause undesired operation of the device.

Radio Frequency (RF) Exposure Compliance of Radiocommunication Apparatus

To satisfy FCC and ISED RF Exposure requirements for mobile devices, a separation distance of 20 cm or more should be maintained between the antenna of this device and persons during operation. To ensure compliance, operation at closer than this distance is not recommended. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.